REMARKS

Claims 1-7 are pending in the subject application, and all of the pending claims stand rejected. By the above amendments, claims 1, 2, and 7 have been amended. Favorable reconsideration of the application and allowance of all of the pending claims are respectfully requested in view of the above amendments and the following remarks.

Claims 2-4 are objected to due to a typographical error in claim 2. Claim 2 has been amended to correct this informality.

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,349,064 to Nakaoka. Applicant respectfully traverses this rejection insofar as it applies to the amended claims.

Claim 1 sets forth an integrated memory comprising a plurality of normal units of memory cells and a plurality of redundant units of memory cells for replacing a defective one of the normal units. The recited integrated memory further includes a memory unit for storing an address of one of the normal units which needs to be replaced, and a comparison unit for comparing an address on an address bus with an address stored in the memory unit and for activating one of the redundant units in the event of a match being identified. As amended, claim 1 further requires a test circuit activated by a test mode signal to reset the memory unit to an initial state and to store an identification code for one of the redundant units in the memory unit for subsequently writing the identification code to the one of the redundant units, wherein the identification code represents a position of the one of the redundant units in the memory cell array, and each of the redundant units is discriminated by a respective identification code. Independent claim 7 sets forth a method for testing an integrated memory and includes analogous limitations.

Thus, amended independent claims 1 and 7 require that a respective identification code by which the redundant units are discriminated from each other and which represents a position of a redundant unit is written to the redundant unit. As explained in Applicant's specification (see, for example, page 7, line 6 to page 8, line 9), the claimed identification code makes it

possible to ascertain which defective normal element is replaced by which redundant element by associating the identification code of a redundant unit to the address of a defective unit. Nakaoka does not disclose or suggest writing an identification code such as an address of the redundant unit in the redundant unit when the semiconductor memory device is operated in the test operational mode, as required by amended claims 1 and 7.

Nakaoka relates to a semiconductor memory device capable of independent selection of normal and redundant memory cells. The semiconductor memory device comprises a memory cell array including a normal memory cell array in which a plurality of normal memory cells are arranged, and a redundant memory cell array in which a plurality of redundant memory cells are arranged for replacing the plurality of normal memory cells. In a test operational mode, the normal memory cell array portion and the redundant memory cell array portion are equally treated in an access operation for the semiconductor memory device, such as read/write, allowing the normal memory cell array portion and the redundant memory cell array portion to be equivalently and successively accessed. To operate the semiconductor memory device in the test operational mode, a test mode signal TM is applied to a spare row decoder 112 with a high level. In the test operational mode, when a redundancy identification address signal RAr is set to a high level, a spare wordline can freely be selected in accordance with a redundancy identification address comprising address signals RA<0:3>. Further, in the test operational mode, when the redundancy identification address signal RAr is at a low level, a normal wordline can be freely selected from an external source in accordance with combinations of row addresses RA<0:3> (see col. 12, lines 5 to 20 of Nakaoka).

Nakaoka discloses a semiconductor memory device by which it is enabled to select a spare wordline in dependence on a redundancy identification address which is applied to a spare wordline selective signal generating circuit 2001 (see Fig. 2 of Nakaoka) or 1400 (see Fig. 7). However, the semiconductor memory device disclosed by Nakaoka does not include anything analogous to the claimed identification code, which allows one to discriminate between the redundant units and ascertain which memory cell in the normal memory cell array is replaced by

which redundant memory cell of the redundant memory cell array. For this purpose, the integrated memory of the present invention is operable in a test mode in which an identification code by which the redundant units are discriminated from each other and which represents a position of the redundant unit in the redundant memory cell array is written to the redundant unit, as recited in claims 1 and 7. According to Nakaoka, in a test operational mode redundant units are selected by a respective redundancy identification address for test purposes without writing the redundancy identification address or a redundancy identification code in the selected redundant memory unit. Consequently, independent claims 1 and 7 and dependent claims 2-6 are not anticipated by Nakaoka; accordingly the Examiner is respectfully requested to reconsider and withdraw the rejection of claims 1-7.

In view of the foregoing, Applicant respectfully requests the Examiner to find the application to be in condition for allowance with claims 1-7. However, if for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to call the undersigned attorney to discuss any unresolved issues and to expedite the disposition of the application.

Applicant hereby petitions for any extension of time that may be necessary to maintain the pendency of this application. The Commissioner is hereby authorized to charge payment of any additional fees required for the above-identified application or credit any overpayment to Deposit Account No. 05-0460.

Respectfully submitted,

Patrick J. Finnan
Registration No. 39,189

EDELL, SHAPIRO & FINNAN, LLC
1901 Research Boulevard, Suite 400
Rockville, Maryland 20850-3164
(301) 424-3640

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